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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,175	06/19/2001	A. Kent Porterfield	303.760US1	2810

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EXAMINER	
AMIN, NIRAV S	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,175	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Nirav S Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-59 are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley et al. (Appl. No.: 09/747,422) herein after referred to as Riley in view of Armstrong, II et al. (Appl. No.: 09/755,658) herein after referred to as Armstrong, II.

As per claim 1, Riley discloses:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register [Page 35, para [0672], [0677]]; and

Riley does not expressly disclose:

a locking mechanism to conditionally make the next node pointer register of each of the plurality of nodes read-only.

Armstrong, II discloses:

a locking mechanism to conditionally make the next node pointer register of each of the plurality of nodes read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 6, Riley discloses:

a hardware implemented capabilities list [Page 35, para [0672], [0677]];

Riley does not disclose:

the list capable of being modified by low-level software, and read-only to higher level software.

Armstrong, II discloses:

the list capable of being modified by low-level software, and read-only to higher level software [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 11, Riley discloses:

an address bus (103);

a data bus (105);

a control bus (109);

a series of linked list registers coupled to the address, data, and control busses, the series of linked list registers arranged in a writeable linked list [Page 35, para [0672], [0677]];; and

Riley does not disclose:

a control register operable to lock the writeable linked list and conditionally make the series of linked list registers read-only.

Armstrong, II discloses:

a control register operable to lock the writeable linked list and conditionally make the series of linked list registers read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 16, Riley discloses:

a plurality of linked lists formed from registers [Page 35, para [0672], [0677]];

a head pointer register to point to one of the plurality of linked lists;

Riley does not disclose:

a control register to conditionally make the head pointer register read-only.

Armstrong, II discloses:

a control register to conditionally make the head pointer register read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 27, Riley discloses:

a plurality of register groups, each register group including registers operable to indicate capabilities of the integrated circuit, and including a next group register to point to a next group [Page 35, para [0672], [0677]];

Riley does not disclose:

a control register operable to render the plurality of register groups read-only.

Armstrong, II discloses:

a control register operable to render the plurality of register groups read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 32, Riley discloses:

a bus (103);

a memory device (140) with basic input output software coupled to the bus;

a peripheral device coupled to the bus, the peripheral device including a capabilities list implemented in groups of registers [Page 35, para [0672], [0677]]; and

a processor (102) to execute instructions in the basic input output software.

Riley does not disclose:

modifying the capabilities list.

Armstrong, II discloses:

a locking mechanism to conditionally make a register read only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 37, Riley discloses:

a PCI local bus compliant peripheral device (122) coupled to a bus; and

a processor (102) coupled to the bus wherein the PCI local bus compliant peripheral device includes a capabilities linked list [Page 35, para [0672], [0677]].

Riley does not disclose:

the capabilities linked list is modifiable by the processor, and wherein the PCI local bus compliant peripheral device further includes a writeable control register operable to render the capabilities linked list read-only by the processor.

Armstrong, II discloses:

a writeable control register operable to render the capabilities linked list read-only by the processor [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 42, Riley discloses:

a control register [Page 35, para [0672], [0677]];

a first list node having a capabilities register and a next node pointer register [Page 35, para [0672], [0677]]; and

a second list node having a capabilities register and a next node pointer register [Page 35, para [0672], [0677]];

Riley does not disclose:

the next node pointer registers of the first and second list nodes are conditionally read-only in response to the control register.

Armstrong, II discloses

a locking mechanism to conditionally make a register read only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 47, Riley discloses:

writing a list of capabilities to nodes in a hardware linked list within the computer peripheral [Page 35, para [0672], [0677]];

Riley does not disclose:

writing to a control register within the computer peripheral to make the nodes read-only.

Armstrong, II discloses:

writing to a control register within the computer peripheral to make the nodes read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 52 Riley discloses:

a capabilities linked list in the PCI local bus compliant device [Page 35, para [0672], [0677]];

Riley does not disclose:

reading instructions from a memory device holding basic input output software;

writing to a control register in the PCI local bus compliant device to make the link read-only.

Armstrong, II discloses:

reading instructions from a memory device holding basic input output software;

writing to a control register in the PCI local bus compliant device to make the link read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 56, Riley discloses:

modifying a next node pointer register in a PCI local bus peripheral to indicate the existence of a capability [Page 35, para [0672], [0677]];

Riley does not disclose:

modifying a control register in the PCI local bus peripheral to make the next node pointer register read-only.

Armstrong, II discloses:

modifying a control register in the PCI local bus peripheral to make the next node pointer register read-only [Page 2, para. [0021], [0022]].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the locking mechanism of Armstrong, II in the system of Riley to conditionally lock the linked list.

As per claim 2, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the locking mechanism comprises a control register.

As per claim 3, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein each of the plurality of nodes includes a register operable to specify a capability of the apparatus.

As per claim 4, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the apparatus comprises a PCI local bus compliant peripheral device.

As per claim 5, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the apparatus comprises an integrated circuit having a microprocessor bus compatible interface.

As per claim 7, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the hardware implemented capabilities list comprises a plurality of list nodes that each include a writeable next node pointer register.

As per claim 8, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a control register coupled to the writeable next node pointer registers, the control register being operable to change the writeable next node pointer registers to read-only next node pointer registers.

As per claim 9, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the hardware implemented capabilities list is writeable by basic input output software and read-only to operating system software.

As per claim 10, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the PCI local bus compliant device comprises an integrated circuit that includes the hardware implemented capabilities list.

As per claim 12, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the series of linked list registers are arranged in groups, each group forming a linked list node, each linked list node including one next node pointer register.

As per claim 13, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is operable to make the next node pointer register of each linked list node read-only.

As per claim 14, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is accessible by a first level of software and the series of linked list registers are accessible by a second level of software, wherein the first level of software is lower than the second level of software.

As per claim 15, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the integrated circuit comprises a PCI local bus compliant computer peripheral.

As per claim 17, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is a write-once register.

As per claim 18, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein each of the plurality of linked lists is formed from linked list nodes, each linked list node includes a writeable next node pointer register.

As per claim 19, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register conditionally makes the writeable next node pointers read-only.

As per claim 20, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is a write-once register.

As per claim 21, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register can be written only once between system resets.

As per claim 23, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register can be written only once between system resets.

As per claim 24, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a hardware linked list pointed to by the second writeable register, the hardware linked list including a plurality of nodes, each of the plurality of nodes comprising a writeable next node register.

As per claim 25, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is operable to make the writeable next node registers read-only.

As per claim 26, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a PCI local bus compliant interface.

As per claim 28, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the plurality of register groups form a PCI local bus compliant capabilities list.

As per claim 29, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is modifiable once by basic input output software, and is not modifiable by operating system software.

As per claim 30, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register comprises a write-once lock bit, that when written, renders the plurality of register groups read-only.

As per claim 31, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the write-once lock bit is configured such that the write-once lock bit can be written to only once between hardware reset sequences.

As per claim 33, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the peripheral device further comprises a control register, that when written to, renders the groups of registers read-only.

As per claim 34, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the memory device includes processor instructions stored therein to write to the control register.

As per claim 35, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the peripheral device includes a PCI local bus compliant interface.

As per claim 36, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include an add-in card upon which the peripheral device resides.

As per claim 38, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the capabilities linked list comprises a plurality of nodes made up of groups of registers, each node corresponding to one capability and including one writeable next node pointer register.

As per claim 39, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the writeable control register is operable to render the writeable next node pointer registers read-only.

As per claim 40, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a memory device having processor instructions stored therein, the processor instructions being operable to cause the processor to write to the writeable control register.

As per claim 41, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the PCI local bus compliant peripheral device includes a writeable register to indicate whether the capabilities linked list is enabled.

As per claim 43, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a writeable head pointer register to point to the first list node, the writeable head pointer register being conditionally read-only in response to the control register.

As per claim 44, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the hardware linked list is compliant with a PCI local bus rev. 2.2 capabilities list.

As per claim 45, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register is a write-once register.

As per claim 46, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the control register can be written to only once between hardware resets.

As per claim 48, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the nodes each include a capability register

and a next node pointer register, and writing a list of capabilities comprises modifying the next node pointer register.

As per claim 49, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein writing to a control register comprises writing once to a capabilities lock bit, which thereafter is read-only.

As per claim 50, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to write to a capabilities list enabled register to signify whether the list of capabilities is enabled.

As per claim 51, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the method is performed by basic input output software prior to loading of an operating system.

As per claim 53, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the capabilities linked list comprises a plurality of nodes, each node including a capabilities register and a next node pointer register, and wherein modifying a link comprises writing to the next node pointer register.

As per claim 54, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to write to a capabilities list enabled register.

As per claim 55, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to write to a head pointer register.

As per claim 57, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the method further comprises modifying a head pointer register to point to a hardware capabilities linked list, wherein the head pointer register becomes read-only responsive to the control register.

As per claim 58, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the apparatus comprises a read-only memory.

As per claim 59, at the time of the invention, it would have been obvious to a person of ordinary skill in the art wherein the method further comprises modifying a capabilities list enabled register, wherein the capabilities list enabled register becomes read-only responsive to the control register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NA

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